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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,629	10/20/2003	Satoshi Inoue	244186US2	1805

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,629	INOUE, SATOSHI	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/03,04/28/05*, 11/01/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 1-20 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-11, 12, 13, 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Dunning et al. (4,145,739).

1. As to claims 1,12, Dunning taught a system (see fig.2) including at least :

a) processor core (see master 16) including a general-purpose register [not explicitly shown] , instruction decoder [command decoder], and a second execution [Intel 8080] (see fig.3 and fig.6 for details);

b) an extension unit (see the workstation) including a first execution unit [8080] connected the processor, and

c) direct memory access controller connected to both the processor core and the extension unit (see the DMA interface both in master in fig.3 and the workstation in fig.5, see also the DMA controller [104][120] in fig.6, see also fig.10) .

2. Dunning did not explicitly show the general purpose register as clamed. However, the examiner holds that general purpose register had been known to be the necessary functional part of the design of a microprocessor in the art, such as the accumulator register in Intel 8080. Since Dunning taught 8080 processor, it must have a general purpose register (e.g. accumulator).

3. As to claims 2, 13, see connection between master 16 and one of the workstation in fig.2.

4. As to claims 7,18, Dunning was also redirected to reconfigurable execution un it (see he hardware status of the slave commands in col.9, lines 1-68, col.10, lines 1-38).

5. As to claims 8, 9, see local memory [24] and control register [418] in fig.5 . See also fig.12 [command decoder] and the control signals of 8080.

6. As to claims 10, 19, see input at DMA interface in fig.14.

7. As to claims 11,20, see output to memory in fig.14.

8. As to the semiconductor chip in claim 12, Dunning's master 8080 was also on a semiconductor chip, such as Intel 8080 (see col.4, lines 60-68).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-6 , 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunning et al. (4,145,739) in view of Intrater et al. (5,822,779).

10. As to claims 3,4,5, 14,15, limitations of parent claims have been given in the paragraph above. Dunning did not specifically show the disable signal circuit to receive the instruction form the decoder to output clock disable signal as claimed. However, Intrater disclosed a system including a decode and control circuit for reset a CPU core (see col.5, lines 25-40). It would have been obvious to one of ordinary skill in the art to use Intrater in Dunning for including the disabling circuit for generating disable output signal as claimed because the use of Intrater could provide Dunning the ability to set and reset the CPU core at a predefined set of decoded command, and it could be achieved by reconfiguring the control parameters of Intrater (e.g. the clock reset) into Dunning so that the specific clock disabling signal of Intrater could be recognized by Dunning, and because Dunning also taught a off/on and reset signal to his CPU (see col.4, lines 14-22), which was a suggestion of the need to disable a CPU core on a decoded command in order to enhance the interface capability of the system control, and in doing so, provided a motivation.

11. As to claims 6,16, Intrater's reset outputted from the decoder and control circuit was applicable as a halt request.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Parkinson et al. (3,976,979) is cited for the teaching of a processor core [host][coupler] and an extension core [remote processor] (see fig.14, col.2, lines 32-57).

b) Anderson et al. (6,594,711) is cited for the teaching of the DMA interface with core processor and extended processor (see fig.4, see also the instruction decoder for details in figs.6,7, col.8, lines 1-68, col.9, lines 1-16).

c) Cheng et al. (5,734,924) is cited for the teaching of the general purpose register and instruction decoder in a processor core (see fig.2B).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP